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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,004	11/02/2001	Allen Gunther	6557-59043	1234

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,004	GUNTHER ET AL.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *23-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 34-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/12/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species of Figures 6-9 in the reply filed on 6/24/2004 acknowledged. The traversal is on the ground(s) that that the alleged species are not independent invention. This is not found persuasive because species of Figures 6-9 are related to a test structure to test tunnel openings, directed to claims 1-22 and 34-39, invention I, while Claims 23-33 are related to a method for testing tunnel openings by charging multiple floating gates and reading multiple sense devices to determine whether charge is stored on the floating gates, invention II.

Inventions I and II are related as product and process of use. The inventions are distinct from each other. In the instant case the method of testing tunnel openings can be practiced with another materially different test structure for testing a semiconductor device having tunnel openings (MPEP § 806.05(h)).

Claims 23-33 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 6/24/2004.

Since Applicant failed to elect the claims directed to species of Figures 6-9 as required by the Restriction in the prior Office Action, the Examiner hereby elects Claims 1-22 and 34-39, for examination.

Specification

2. The abstract of the disclosure is objected to because it fails to comply with the proper language and format for an abstract of the disclosure. On line 1, the word "disclosed" should be deleted. The abstract exceeds 150 words (actual word count is 229).

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9, 12-16, 21, 22 and 34-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Asano et al. (US Patent NO: 5,323,039, issued: June 21, 1994).

Regarding independent Claim 1, Asano discloses a non-volatile semiconductor memory, comprising:

Multiple write paths (word lines WL1-WL7) aligned in parallel, as shown in Figures 10A, 10B and Figure 11, which is an equivalent circuit for Figure 10A of a pattern of one embodiment.

An oxide layer films (12, 12....) adjacent to the write paths (WL1-WL7), as shown in Figures 1B and 10B.

An array of tunnel openings 42 formed in the oxide layer 12, the array having multiple rows and columns of multiple tunnel openings, Figures 16A and 16B.

Wherein at least one of the columns in the array of tunnel openings 42 is electrically coupled with a single write path (WL1-WL7).

Regarding Claim 2, Asano discloses wherein the array of tunnel openings 42, Figures 16A and 16B, is of size NXM, where N=8 is the number of write paths and M=8 is the number of floating gates, then NXM=64.

Regarding Claim 3, Asano discloses wherein at least one of the floating gates 16 is aligned to a subset of tunnel openings 42 to write data into memory cells (52-59) corresponding to (WL1-WL7) to allow programming and erasing of multiple floating gates in parallel, using erase gates 72 connected to erase gate lines EGL1 and EGL2 for applying erase gate line signals

Regarding Claim 4, Asano discloses wherein each path (word lines WL1-WL7) is electrically coupled to the multiple floating gates 16, through multiple tunnel openings 42, Figures 11 and 16A.

Regarding Claim 5, Asano discloses wherein there is a one-to-one correspondence between tunnel openings 42 in the write path WL1 and the floating gates 16, Figures 11 and 16A.

Regarding Claim 6, Asano discloses wherein at least a first floating gate 16 is electrically coupled to multiple tunnel 42 openings so that the first floating gate is separately programmable and erased through any one of the multiple tunnel openings, Figures 11 and 16A.

Regarding Claim 7, Asano discloses wherein the multiple floating gates 16 are positioned perpendicular to multiple write paths (WL1-WL7) and wherein a tunnel opening 42 is located at each floating gate 16 and write path intersection, Figures 11 and 16A.

Regarding Claim 8, Asano discloses a control path such as erase gate lines EGL1 and EGL2 connected to erase gates 72 and aligned perpendicularly to and coupled to the multiple floating gates 16 to control programming and erasing the multiple floating gates by applying erase gate line signals EG1 and EG2, Figure 11.

Regarding Claim 9, Asano discloses a read path comprising a sense amplifier (not shown) that are turned ON with the floating gates programmed and that are turned OFF with the floating gates erased connected to the data line (DL1) aligned perpendicularly to and coupled to the multiple floating gates to form a series of sense transistors for sensing data from memory cells (32-39), Figure 2.

Regarding independent Claim 12, Asano discloses a non-volatile semiconductor memory, comprising:

Multiple write paths (word lines WL1-WL7) aligned in parallel, as shown in Figures 10A, 10B and Figure 11, which is an equivalent circuit for Figure 10A of a pattern of one embodiment.

Multiple floating gates (16, Figure 10A) aligned in parallel and aligned perpendicularly to the multiple write paths (WL1-WL7), the floating gates (16) overlapping the multiple write paths to form an array of intersecting areas where the overlap occurs (Figure 11).

An array of tunnel openings (42) formed in the intersecting areas of overlap, Figures 16A and 16B.

And wherein at least one of the write paths (word lines WL1-WL7) is electrically coupled to the multiple floating gates (16) through multiple of the tunnel openings (42) to write data into memory cells (52-59) corresponding to (WL1-WL7) to allow programming and erasing of multiple floating gates in parallel, using erase gates 72 connected to erase gate lines EGL1 and EGL2 for applying erase gate line signals. In the memory constructed as above, data are erased by setting WL1 to WL8 all to 0 V, and EG1 (or EG2) to 20 V. Electrons as Fowler-Nordheim's tunnel current are therefore emitted from the floating gates 16 of the memory cells 52 to 59 connected to the gate line EGL1 (or EGL2), to the erase gate 72 to thereby erase data, Figures 10 and 11.

Regarding Claim 13, Asano discloses wherein one tunnel (42) opening is formed in each intersecting area of overlap, Figure 16A.

Regarding Claim 14, Asano discloses wherein each path (word lines WL1-WL7) is electrically coupled to the multiple floating gates 16, Figure 11.

Regarding Claim 15, Asano discloses a read path comprising a sense amplifier (not shown) connected to the data line (DL1) aligned perpendicularly to and coupled to the multiple floating gates to form a series of sense transistors for sensing data from memory cells (32-39), Figure 2.

Regarding Claim 16, Asano discloses a control path such as erase gate lines EGL1 and EGL2 connected to erase gates 72 and aligned perpendicularly to and coupled to the multiple floating gates 16 to control programming and erasing the multiple floating gates by applying erase gate line signals EG1 and EG2, Figure 11.

Regarding independent Claim 21, Asano discloses a non-volatile semiconductor memory, comprising:

Multiple write paths (word lines WL1-WL7) aligned in parallel, as shown in Figures 10A, 10B and Figure 11, which is an equivalent circuit for Figure 10A of a pattern of one embodiment.

An oxide layer films (12, 12....) adjacent to the write paths (WL1-WL7), as shown in Figures 1B and 10B.

An array of tunnel openings 42 formed in the oxide layer 12, the array having multiple rows and columns of multiple tunnel openings, Figures 16A and 16B.

Wherein at least one of the columns in the array of tunnel openings 42 is electrically coupled with a single write path (WL1-WL7).

Regarding Claim 22, Asano discloses plurality of floating gates 16, wherein at least one row in the array of tunnel openings is electrically coupled to a single floating gate 16, Figures 16A, 10A and 11.

Regarding independent Claim 34, Asano discloses a non-volatile semiconductor memory, comprising:

Means (word lines WL1-WL7) for programming multiple floating gates (16) in parallel, by writing data in memory cells (52 to 59), described as follows: "for example, the word line WL1 is set to 12 V, data line DL to 10 V, select gate signals SG1, SG3 and SG4 to 20 V, and non-selected word lines WL2 to WL8 to 20 V. Electrons are therefore injected into the memory cell 52 by means of the hot electron effect, to thereby write data. In writing data into the memory cell 53, word line WL2 is set to 12 V while setting other word lines WL1, WL3 to WL8 to 20 V. In a similar manner, up to the memory cell 59 data can be sequentially written", Figures 10 and 11.

Means for reading using a sense amplifier (not shown) connected to the data line (DL1) aligned perpendicularly to and coupled to the multiple floating gates 16 to form a series of sense transistors for sensing data from memory cells (32-39), Figure 2, to verify the multiple floating gates 16 are properly programmed.

Means for erasing the multiple floating gates using means erase gates 72 connected to erase gate lines EGL1 and EGL2 for applying erase gate line signals, where data in the memory are erased by setting WL1 to WL8 all to 0 V, and EG1 (or EG2) to 20 V.

Regarding Claim 35, Asano discloses means such as write paths (word lines WL1-WL7) for electrically coupled to the multiple floating gates (16) through multiple of the tunnel openings (42) to write data into memory cells (52-59) corresponding to (WL1-WL7) to allow programming and erasing of multiple floating gates in parallel, using erase gates 72 connected to erase gate lines EGL1 and EGL2 for applying erase gate line signals

Regarding Claim 36, Asano discloses means (word lines WL1-WL7) for electrically coupling the single write path to multiple same-size tunnel openings 42, Figure 16A.

Regarding independent Claim 37, Asano discloses a non-volatile semiconductor memory, comprising:

An array of tunnel openings (42) aligned in rows and columns, Figures 16A and 16B.

Multiple floating gates (16, Figure 10A) electrically coupled to the rows of tunnel openings 42, and aligned with the multiple write paths (WL1-WL7), the floating gates (16) overlapping the multiple write paths to form an array of intersecting areas where the overlap occurs (Figure 11).

Multiple write paths (word lines WL1-WL7), which are electrically coupled to the columns of tunnel openings 42, Figures 16A and 16B.

Regarding Claim 38, Asano discloses wherein the tunnel openings 42 in a first column of the array are of the same size means size and wherein a first write path

(word lines WL1-WL7) is electrically coupled to multiple same-size tunnel openings 42, Figure 16A.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10, 11, 17-20 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (US Patent NO: 5,323,039, issued: June 21, 1994) in view of Chang et al. (US Patent NO: 5,273,923, issued: December 28, 1993).

Regarding Claims 10, 11, 17-20, 39, Asano substantially discloses an array including rows and columns of tunnel openings 42, and wherein any of the columns have same size tunnel openings formed in the intersecting areas, Figures 16A and 16B.

Asano does not explicitly disclose, the claimed limitations, "wherein the tunnel openings associated with the write paths vary in size" and wherein "different size of tunnel opening associated with each column from other columns in order to test varying sizes of tunnel openings", and "wherein a first write path is associated with a one-dimensional array of a first size tunnel opening and a second write path is

associated with a one dimensional array of a second size tunnel opening, which differs in size from the first size", and "wherein a first floating gate is electrically coupled to multiple tunnel openings designed to have varying sizes", and "wherein the set of tunnel openings is of varying size so that different size tunnel openings can be tested".

However, in analogous art, Chang discloses, Figure 1, a process for fabricating an EEPROM cell including the method steps of defining a tunnel area (30) by the length of the tunnel opening 28 and the width of active region 12, which overlaps the tunnel opening, where the minimum tunnel area is determined by the smallest dimension of the tunnel opening and the smallest dimension of the active region. Accordingly, tunnel area adjustments are made by modifying the dimensions of the tunnel opening, the active region, or both.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the method steps of adjusting the dimensions of tunnel opening as taught by Chang, in the non-volatile semiconductor memory of Asano, for the purpose of determining the minimum tunnel area. A person skilled in the art would have been motivated to modify Asano, since Chang' method enables an EEPROM cell to have a minimal tunnel area for improved performance, without necessitating overly complex fabrication techniques. In addition to having reduced process complexity, Chang' method also results in an increase in the capacitance coupling ratio, thereby improving performance over conventional EEPROM devices.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Office Action: Non-Final Rejection

By:

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